COMMENTS

This Amendment is submitted in response to the Office Action dated March 24, 2006, having a shortened statutory period set to expire June 26, 2006. In the present Amendment, Claims 1-2, 5-6 and 9-10 are amended, Claims 13-16 are cancelled, and Claims 17-20 are added. Upon entry of the proposed amendments, Claims 1-12 and 17-20 are now pending.

Rejections under 35 U.S.C. § 102 and 103

In paragraph 4 of the present Office Action, the Examiner has rejected Claim 1 under 35 U.S.C. § 102(b) as being anticipated by *Takashima et al.* (U.S. Patent No. 6,347,372 – "*Takashima*"). In paragraph 6 of the present Office Action, the Examiner has rejected Claims 5, 9 and 13 under 35 U.S.C. § 103(a) as being unpatentable over *Takashima* in view of *Dove et al.* (U.S. Patent No. 5,938,765 – "*Dove*"). In paragraph 12 of the present Office Action, the Examiner has rejected Claims 2, 6, 10 and 14 under 35 U.S.C. § 103(a) as being unpatentable over *Takashima* in view of *Dove*. In paragraph 15 of the present Office Action, the Examiner has rejected Claims 3, 7, 11 and 15 under 35 U.S.C. § 103(a) as being unpatentable over *Takashima* in view of *Dove* and further in view of *Stallmo et al.* (U.S. Patent No. 5,689,678 – "*Stallmo*"). In paragraph 19 of the present Office Action, the Examiner has rejected Claims 4, 8, 12 and 16 under 35 U.S.C. § 103(a) as being unpatentable over *Takashima* in view of *Dove* and further in view of *Golden et al.* (U.S. Patent No. 6,681,282 – "*Golden*"). Applicants respectfully traverse these rejections in light of the present amendment.

With regards to exemplary Claim 1, which is now amended to include the features of originally filed Claim 2, the cited art does not teach or suggest "wherein the scalability chipset comprises a local memory controller for a booting node in the plurality of processor nodes, instructions for processor allocation and set-up of hardware/software in the booting node, and host bridge controller information for the booting node," as supported in the present specification at paragraph [0014]. *Dove* is cited, in paragraph 14 of the present Office Action, for teaching a "host bridge controller" in each processor node, but not in a scalability chipset in a scalability management module (SMM). The Examiner states that it "would have been obvious to one of ordinary skill to have a host bridge controller within the scalability chipset rather than each

processor node." First, it is a primary function of the present invention to permit the SMM to reconfigure a multi-node computer if one of the nodes fails (see paragraph [0008] of the present specification). If the host bridge controller was only in the nodes, then the invention would not work as optimally described and disclosed. Second, the cited art does not teach or suggest a scalability controller that includes "instructions for processor allocation and set-up of hardware/software in the booting node." The "scalability controller" cited in original Claim 2 is *Takashima's* processor-status detection unit (P/SD) 35, which detects boot statuses such as boot request status, processor description, boot type, boot length, boot speed, boot completion and block transmission result (*Takashima* col. 7, lines 26-37). There is not teaching or suggest found in the combination of the cited art for "instructions for processor allocation and set-up of hardware/software in the booting node." Thus, Applicants respectfully request that Claims 1, 5 and 9 be allowed.

With regards to exemplary Claim 2, as newly amended, the combination of the cited art does not teach or suggest "wherein the scalability chipset in the scalability management module is capable of selectively configuring each processor node, in the coordinated multi-node computer, as a host node, a secondary node, or a hot spare node," as supported in the present specification at paragraphs [0015] and [0020]. Thus, Applicants respectfully request that Claims 2, 6 and 10 be allowed.

Regarding exemplary Claim 3, the combination of the cited art does not teach or suggest "wherein the plurality of processor nodes includes a hot spare node capable of being configured by the scalability management module if another of the processor nodes fails or is removed from the multi-node computer." The Examiner cites *Stallmo* for the teaching of the use of a hot spare hard drive in a RAID configuration. The Examiner's position is that, since each hard drive includes a processor controller, then each hard drive is essentially the same as a node in a multi-processor computer system. Applicants respectfully disagree. To equate a RAID system with a multi-processor computer system violates the guidance found in Section 2143.01 of the MPEP. Specifically, "although a prior art device (*processors found in a RAID system)* 'may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so'" (*comments in italics made by Applicants*). That is, there is

no suggestion found in the cited art to modify a RAID system to the extent that mass storage controllers, that are "optimized for inter-processor communications control and management" in a RAID configuration, could be modified to create a multi-processor computer system. In an effort to amplify the difference, exemplary new Claim 17 includes the clarification that the hot spare node does not include a mass storage device, as supported by Figures 1 and 2 of the present specification. While Applicants are normally hesitant to use negative limitation language, the language of Claim 17 is believed to comport with the rule found in *In re Wakefield*, 422 F.2d 897, 164 USPQ 636 (C.C.P.A. 1970), since the scope of the claim is still definite since the negative limitation (i.e., the node is not a mass storage device) is definite. Applicants therefore respectfully request that Claims 3, 7 and 11 be allowed.

New Claim 20

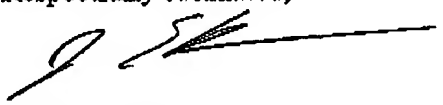
With regards to newly added Claim 20, the combination of the cited art does not teach or suggest the claimed features, which are supported by Figure 3 and paragraphs [0017] to [0024] of the present specification. Therefore, Applicants respectfully request that Claim 20 be allowed.

CONCLUSION

Applicants now respectfully request a Notice of Allowance for all pending claims.

No extension of time for this response is believed to be necessary. However, in the event an extension of time is required, that extension of time is hereby requested. Please charge any fee associated with an extension of time as well as any other fee necessary to further the prosecution of this application to **IBM CORPORATION DEPOSIT ACCOUNT No. 50-0563.**

Respectfully submitted,



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